Micromachined Filters on Synthesized Substrates

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***Abstract*—Effective high-frequency spectrum usage requires high-performance filters to have a sharp cutoff frequency and high stopband attenuation. Stepped-impedance low-pass designs achieve this function best with large ratios of high-to-low-impedance values. In high-index materials, such as Si (11.7) and GaAs (12.9), however, these high-to-low-impedance ratios are around five, thereby significantly limiting optimum filter performance. This paper characterizes the use of Si micromachining for the development of synthesized substrates, which, when utilized appropriately, can further reduce the low-impedance value or increase the high-impedance value. Both designs have demonstrated high-to-low-impedance ratios that are 1.5–2 times larger than conventional techniques.**

***Index Terms*—Filters, micromachining, synthesized substrates.**

I. Introduction

EFFICIENT frequency spectrum usage is required by a variety of communications related applications (e.g., wireless systems, collision avoidance radars, etc.) and demands the development of high-performance filters for frequency selectivity. In addition, the need for highly portable and inexpensive components encourage the development of planar designs on high-index semiconductor materials that offer low-cost manufacturing capability. Good planar filter designs use equivalent transmission-line representation for inductive and capacitive filter elements that result in large high-to-low-impedance ratios. Although high dielectric-constant semiconductor materials (e.g., GaAs and Si) offer compactness, some designs, such as the stepped impedance filter, can suffer from shallow rolloff and poor attenuation in the stopband due to impedance range limitations that preclude achieving large high-to-low-impedance ratios.

In this paper, a silicon (Si) wafer is micromachined to form a "synthesized substrate" that can minimize low impedance and maximize high-impedance values. Preliminary findings of this micromachining approach have been demonstrated in [1] on a stepped-impedance low-pass filter design. Similar designs have been shown in [2], where a BCB polymer membrane technology has been used as an alternative method to semiconductor membrane processing techniques. In this paper, emphasis is placed the use of bulk Si micromachining to achieve optimum filter design.

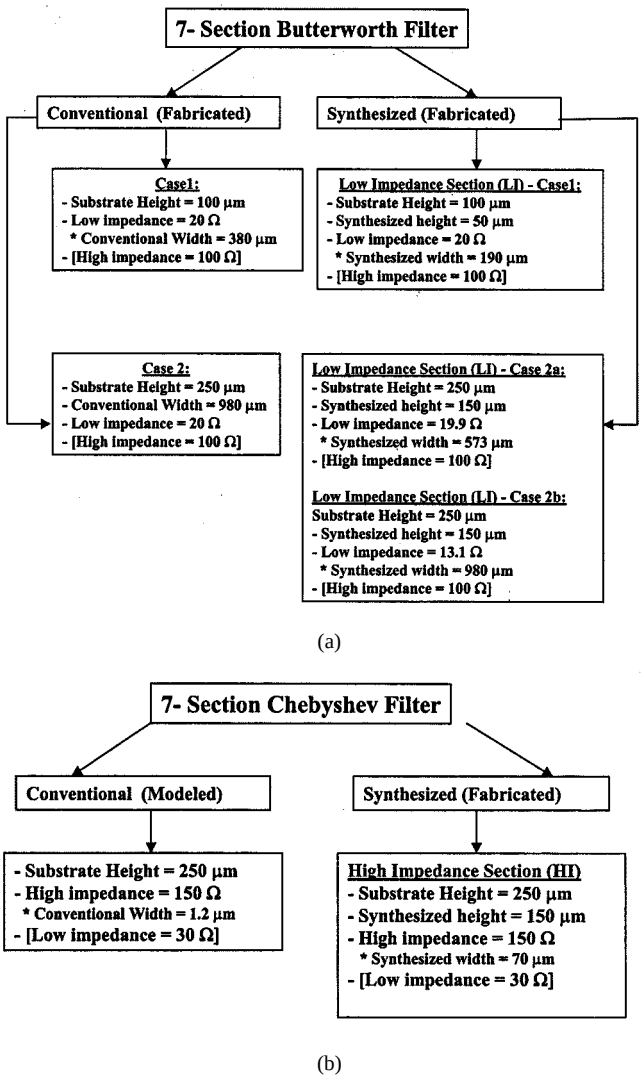

Fig. 1. Micromachined filter design flowchart using the: (a) low-impedance and (b) high-impedance approach. [] denotes the line printed on the full-thickness section of substrate.

Two approaches have been investigated for the development of high-performance micromachined low-pass filters. The first approach attempts to further decrease the low-impedance value of the microstrip line by thinning the substrate locally; whereas, the second one aims at further increasing the high-impedance values by micromachining an air cavity locally to reduce the effective dielectric constant. For comparison purposes, a stepped-

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TABLE I
SYNTHESIZED LOW-IMPEDANCE (LI) DESIGN PARAMETERS FOR FILTER IMPLEMENTATION, WHERE d_{FT} IS THE FULL THICKNESS (FT) HEIGHT, d IS THE MICROMACHINED HEIGHT, AND w IS THE CONDUCTOR WIDTH

Filter Section	Impedance (ohms)	Length (μm)	FT Width (d_{FT}=100 μm; w/d=3.8)	LI-Design 1 Width (d=50 μm)	FT Width (d_{FT} =250 μm; w/d = 3.9)	LI-Design 2a Width (d=150 μm; w/d = 3.82)	Impedances (Ohms)	LI-Design 2b Width (d=150 μm; w/d=6.53)
L1	100	135	10	10	25	25	100	25
L2	20	270	380	190	980	573	13	980
L3	100	684	10	10	25	25	100	25
L4	20	480	380	190	980	573	13	980
L5	100	684	10	10	25	25	100	25
L6	20	270	380	190	980	573	13	980
L7	100	135	10	10	25	25	100	25

impedance filter is used as a demonstration circuit and has been realized on both conventional and synthesized substrates, as outlined in Fig. 1.

II. DESIGN CONSIDERATION AND APPROACH

A. Synthesized Low-Impedance Design Approach

This approach attempts to reduce the low-impedance value in the stepped-impedance filter design in order to increase the high-to-low-impedance ratio using silicon micromachining. To develop impedance values below 20 Ω on high-index materials such as silicon, linewidths must increase substantially for a moderate reduction in characteristic impedance. Furthermore, these large widths contribute to higher radiation loss due to the large step discontinuity between the high- and low-impedance lines. In this approach, the following two objectives were sought: 1) the demonstration of a micromachined filter with increased low-to-high-impedance ratio in comparison to a conventional filter and 2) the identification of important design parameters for the reduction of characteristic impedance values.

Typical microstrip characteristic impedance values (Z_0) on Si ($\varepsilon_r = 11.7$) range from 20 to 100 Ω. The use of micromachining in this design further reduces the low characteristic impedance ($Z_{0,\mathrm{LOW}}$) by locally reducing the substrate height and, as a result, increases the line capacitance. A seven-section high–low Butterworth filter has been designed using Advanced Design System (ADS) and Linecalc[1] and is realized in two configurations. One configuration is the reference design on a standard full-thickness silicon substrate, while the other is the proposed design on a micromachined silicon wafer. This micromachined design realizes low-impedance microstrip 20-Ω sections on a locally thinned 50-μm region, while maintaining the high-impedance microstrip lines on full-thickness Si material (200 μm). An illustration of the layout and circuit dimensions are shown in Fig. 2 and Table I, respectively.

In addition to the specific filter configuration described above, a parametric study of a low-pass micromachined filter with low-impedance sections on 150-μm locally thinned sections is performed to determine the effect of the microstrip width (w) to substrate thickness (d) ratio on filter performance. The results of each design are discussed in detail in the results portion of this paper.

[1]Agilent Technologies Inc., Santa Clara, CA.

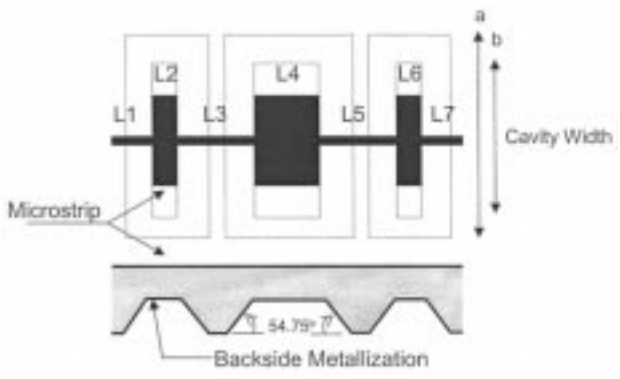


Fig. 2. Circuit layout for micromachined filter on synthesized low-impedance substrate. (top) Stepped impedance microstrip electrode, where individual L_i sections have dimensions indicated in Table I. Dotted lines represent the micromachined cavity region underneath the low-impedance conductor whose widths a and b are listed in Table IV. (bottom) Cross section of the micromachined silicon substrate.

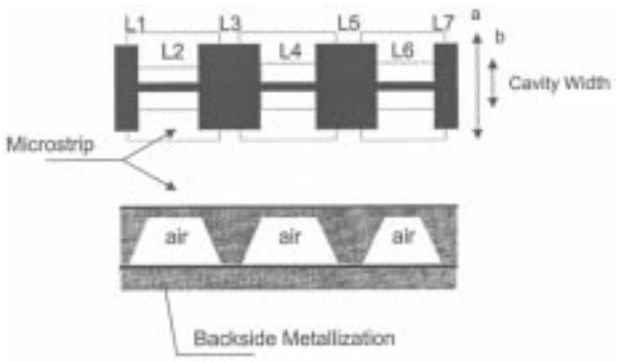


Fig. 3. Circuit layout for micromachined filter on synthesized high-impedance substrate. (top) Stepped-impedance microstrip electrode layout, where individual L_i sections have dimensions indicated in Table II. Dotted lines represent the etched cavity region underneath the high-impedance conductor whose widths a and b are listed in Table IV. (bottom) Cross section of the micromachined silicon substrate.

B. Synthesized High-Impedance Design Approach

This approach attempts to increase the high-impedance value in order to produce a larger high-to-low-impedance ratio. Impedance values above 100 Ω on high-index materials such as Si require linewidths smaller than 10 μm, thus resulting in high ohmic losses. Additionally, the large geometric step discontinuities between the high- and low-impedance sections introduce large parasitics, which are difficult to incorporate

TABLE II
SYNTHESIZED HIGH-IMPEDANCE (HI) DESIGN PARAMETERS ON FULL THICKNESS SILICON AND MICROMACHINED HIGH-IMPEDANCE SECTIONS BASED ON A 10% : 90% RATIO OF Si — AIR REGIONS, WHERE FT IS THE FULL-THICKNESS SUBSTRATE AND h IS THE FULL THICKNESS HEIGHT

Filter Section	Impedance (Ohms)	FT Width (h=250 μm)	FT Length (μm)	HI Width (10:90), (μm)	HI Length (μm)
L1	30	500	268	500	268
L2	150	1.2	271	70	498
L3	30	500	500	500	500
L4	150	1.2	327	70	600
L5	30	500	500	500	500
L6	150	1.2	271	70	498
L7	30	500	268	500	268

into practical filter design iterations. The primary objective in this section is to demonstrate that micromachining can provide a more practical method for realizing very large impedance lines (as high as 150 Ω) without introducing high ohmic losses.

This high-impedance design approach increases the characteristic impedance ($Z_{o,\,\mathrm{HIGH}}$) by locally reducing the effective dielectric constant and, thus, increases line inductance. Fig. 3 and Table II illustrate the layout and dimensions, respectively, for a seven-section 0.5-dB equiripple Chebyshev low-pass filter. Theoretical calculated values of the effective dielectric constant and characteristic impedance of the microstrip lines shown in Figs. 4 and 5 are determined from data generated by a parallelized full-wave FEM simulation tool based on tetrahedral elements [3], [4]. The high-impedance (150 Ω) inductive sections are printed on a 250-μm-thick Si substrate that has been etched locally to create a 220-μm air cavity region underneath the line. This results in an effective dielectric constant of 1.83 (see Fig. 6). The low-impedance (20 Ω) capacitive section remains on full-thickness silicon with an effective dielectric constant equal to 6.153.

C. Capacitance and Open-End Effects in Synthesized Substrate Regions

The capacitance of a transmission line is the sum of the primary line capacitance and the parasitic open-end capacitance. The line capacitance in the micromachined sections is computed from a static model $C = \varepsilon A/d$, where ε is the effective dielectric constant, A is the area, and d is the electrode separation distance. In this analysis, the assumptions are vertical cavity sidewalls and a fixed substrate height. The phase velocity in the reduced height section is reduced when compared to the full-thickness ones due of the increase in capacitance. In contrast, the phase velocity in the reduced dielectric-constant section is increased as a result of the decrease in capacitance. Hence, such variations will cause the micromachined filter design to experience a shift of the 3-dB cutoff frequency compared to the conventional approach.

The open-end capacitance is a function of the substrate thickness, the width of the microstrip line, and the effective dielectric constant of the rest of the substrate. In the micromachined filter design, the parasitic open-end effect [5], which can be represented by the equivalent transmission-line length computed in Table III, is dominated by parasitic radiation that can compromise filter performance considerably. Since capacitance is determined by electrode area and separation, this parasitic radiation effect can also be described by a ratio of conductor width (w) and micromachined substrate height (d). Values of w/d lower than the conventional full thickness w/d result in reduced open-end effect capacitance and must be accounted for in the design on the synthesized substrate.

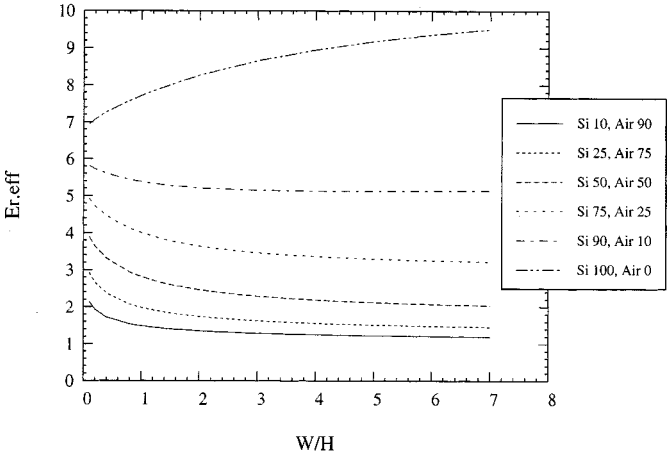


Fig. 4. Effective dielectric-constant data for synthesized high-impedance substrates using air–silicon combinations.

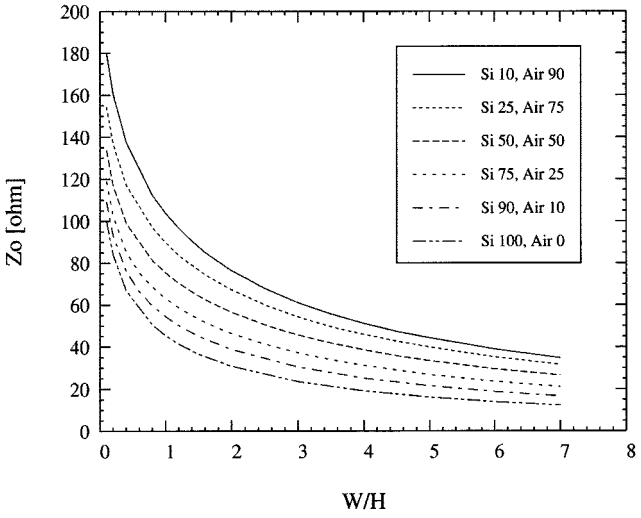


Fig. 5. Characteristic impedance for synthesized high-impedance substrates using air–silicon combinations.

TABLE III
OPEN-END EFFECT CALCULATIONS ARE BASED ON EQUATIONS IN [5] AT 20 GHz, AND ASSUME CONSTANT SUBSTRATE THICKNESS OF 100 μm FOR THE FIRST TWO TYPES AND 200 μm FOR THE REMAINDER

Type	Conductor Width (μm)	Substrate Height (μm)	Effective Dielectric Constant	Characteristic Impedance (Ω)	Off-set Length (μm)
Full thickness	380	100	9.18	19.95	36
LI-Design 1	190	50	9.05	19.50	18
Full Thickness	980	250	9.64	19.67	91
LI-Design 2a (w/d=3.82)	573	150	9.28	19.19	55
LI-Design 2b (w/d = 6.53)	980	150	9.99	13.13	59

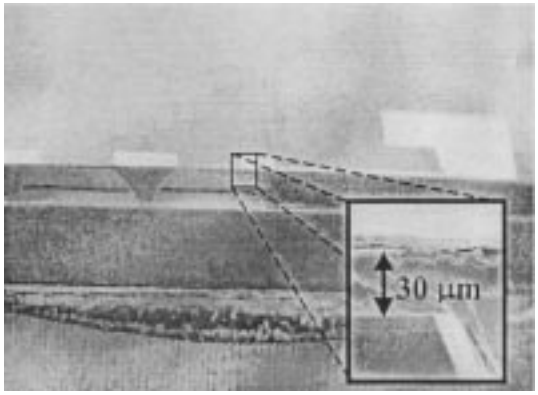


Fig. 6. SEM micrograph of synthesized high-impedance section filter. Inset figure of high-impedance section of line.

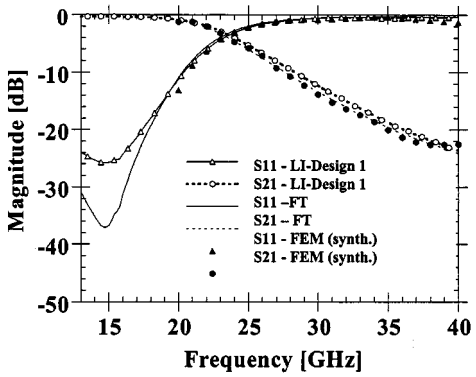


Fig. 7. Seven-section Butterworth filter design. (a) Return-loss ($S11$) and insertion-loss ($S21$) comparison of conventional full-thickness (FT) design to synthesized low-impedance (LI) design 1 on 100-μm-thick silicon.

III. RESULTS AND DISCUSSION

A. General Fabrication Approach and Testing Methodology

All circuits are printed on high-resistivity silicon (1500 $\Omega \cdot$cm) and material is etched locally underneath the desired line to a specific depth using wet anisotropic etchants, e.g., potassium hydroxide (KOH) and tetra methyl ammonium hydroxide (TMAH) [6]. Both chemicals use crystal plane selectivity and form pyramidal cavities with sidewalls angled at 54.75°, as indicated in Fig. 2 and Table IV. The circuits are fabricated with approximately 3.5 μm of electroplated gold (Au) and have approximately 2.5 μm of sputtered titanium–gold (Ti–Au) on the back of the wafer to form the ground plane. In the final stage, each circuit wafer is attached to a metallized support wafer of similar metal composition using conducting silver epoxy[2] to insure ground-plane equalization between the vias and lower metallization.

A Cascade Microtech Probe station and an HP 8510C Network Analyzer are used to measure the filter performance. The thru-reflect-line (TRL) calibration software MULTICAL,[3] [7] is used to eliminate the effects of the 150-μm air coplanar-waveguide ground–signal–ground probe tips and the feedline effects from the measured filter response. The results of these measurements are described in the following sections.

[2]Epoxy Technology Inc., Billerica, MA.

[3]R. B. Marks, D. F. Williams, Program MultiCal, rev. 1.00, National Institute of Standards (NIST), Boulder, CO, Aug. 1995.

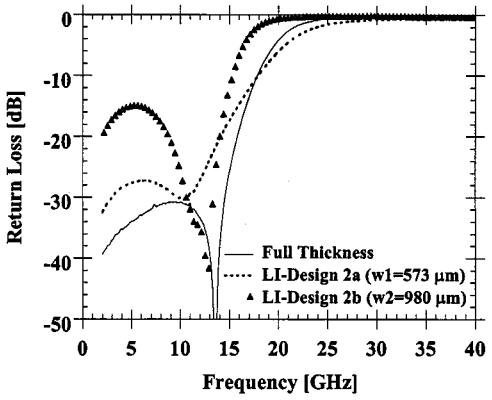
B. Synthesized Low-Impedance Design Results

Two different design approaches have been applied to a seven-section Butterworth filter design, and measured data of each are compared to a conventional full-thickness reference filter. One design attempts to validate the micromachining approach by realizing the 20-Ω low-impedance sections of the conventional design onto the micromachined 50-μm-thick substrate areas. These capacitive sections are represented by 190-μm-wide lines that maintain the w/d ratio of the conventional design (3.8). The synthesized design compares well to the reference (Fig. 7), having a 3-dB cutoff frequency of 20.5 GHz and, thus, confirming the accuracy of the approach.

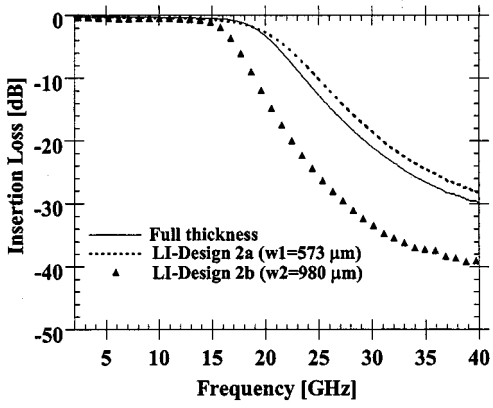
In the other design approach, the effects of varying the conventional design w/d ratio value is studied for lower impedances realized on micromachined 150-μm-thick substrate areas. Minor changes in the conventional w/d value (3.9) are obtained by reducing the linewidth on the micromachined area. The resulting w/d ratio (3.82) shows negligible change in the characteristic impedance value. This minor change does, however, cause the 3-dB cutoff frequency to shift upward due to the net reduction in the primary line and open-end capacitance, and is shown in Fig. 8 as "LI-Design 2a." Changes in the conventional w/d ratio to values greater than a factor of 1.5 (6.53) are obtained by maintaining the full-thickness conductor width while reducing the substrate height. This adjustment leads to a substantial reduction in the micromachined low-impedance value (13 Ω) and causes the 3-dB cutoff frequency, shown in Fig. 8 as

TABLE IV
PYRAMIDAL CAVITY WIDTHS AT TOP AND BOTTOM OF MACROMACHINED CAVITY, WHERE FT DENOTES THE FULL THICKNESS DESIGN

Design Type	FT height (μm)	Lower cavity width, a (μm)	Upper cavity width, b (μm)
Low Impedance	100	1385	1323
Low Impedance	250	3480	3338
High Impedance	250	570	270



(a)



(b)

Fig. 8. Seven-section Butterworth filter design. (a) Return- and (b) insertion-loss comparison of conventional full-thickness design and synthesized low-impedance (LI) designs 2a ($w/d = 3.82$) and 2b ($w/d = 6.53$) on 250-μm-thick silicon substrate.

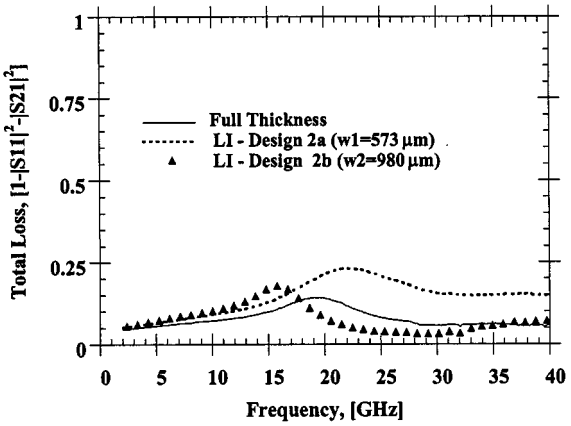


Fig. 9. Seven-section Butterworth filter design comparison between conventional full-thickness and synthesized low-impedance (LI) designs 2a ($w/d = 3.82$) and 2b ($w/d = 6.53$) on 250-μm-thick silicon substrate.

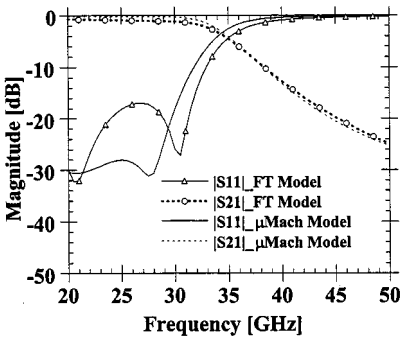


Fig. 10. Seven-section Chebyshev filter response. Theoretical return ($S11$) and insertion ($S21$) loss of high-impedance filter design model on full-thickness (FT) silicon substrate and on micromachined (μMach) substrate using Advanced Design System. See Table II for dimensions.

"LI-Design 2b," to shift to much lower frequencies (16.5 GHz) as a result of an increase in primary capacitance.

Fig. 9 shows a comparison of the loss between the various micromachined cases and indicates that a narrow-band peak near cutoff for the high w/d value (6.53) is due to the steeper slope in the return-loss response. This steeper slope can be attributed to an increase in the high-to-low-impedance ratio from 5 to 7.5 in the 13-Ω design, which has been confirmed by ADS simulations. A 10-dB improvement is also observed in Fig. 8(b) in the rejection band compared to the 20-Ω designs. Therefore, reduction of the characteristic impedance in the capacitive sections of *L-C* filter produces sharper rejection band edge in a low-pass design.

C. Synthesized High-Impedance Design Results

A seven-section Chebyshev low-pass filter design is investigated using 150-Ω high-impedance lines for the inductive sections of the *L-C* circuit. As discussed in the design section, the impracticality of fabricating such high impedances resulted in simulation data only of the reference design on the full-thickness silicon substrate. A similar ADS model has been developed for the micromachined design in which high-impedance lines are printed on locally reduced effective dielectric-constant regions. The simulation results are shown in Fig. 10 for models, where a lossless substrate is assumed with finite metallization

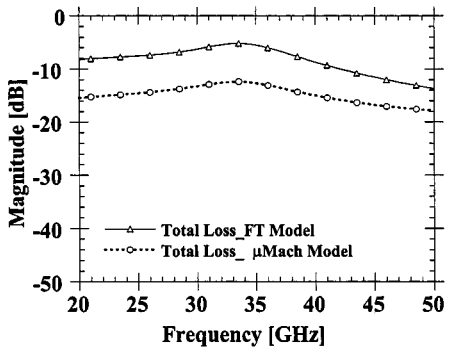


Fig. 11. Seven-section Chebyshev filter response. Total loss ($1 - |S11|^2 - |S21|^2$) calculations for the high-impedance filter design on full-thickness (FT) and micromachined (μMach) substrate based on ADS simulations.

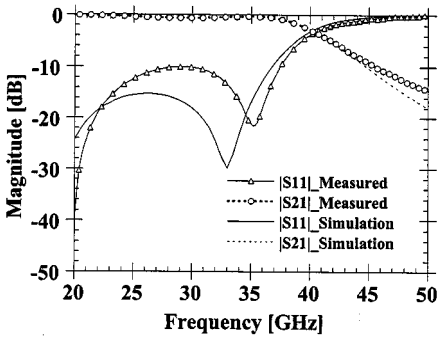


Fig. 12. Seven-section Chebyshev filter response. Measurement data for synthesized high-impedance filter design 250-μm-thick silicon substrate.

thickness (3.5 μm). This reduced geometric effective dielectric-constant approach offers several advantages. First, it reduces the geometric step-discontinuity ratio between the high- and low-impedance sections from 416 in the impractical conventional design to seven in the micromachined one (see Table II). Second, the increase in conductor width for the simulated micromachined case, as seen in Fig. 11, shows substantially reduced losses, at least 4 dB lower than the conventional design primarily due to lower current density.

The realized micromachined filter design has the inductive sections printed on a reduced effective dielectric-constant region localized at the positions of the air cavities (see Fig. 3). The air cavities are pyramidal in shape and have top and bottom widths equal to 270 and 570 μm, respectively, for corresponding lengths indicated in Table II for the high-impedance filter design. From simulations, the filter response is observed to depend on the shape and size of the cavity. In test cases, the design filter was simulated with vertical walls corresponding to either 270- or 570-μm widths and were observed to have a 3-dB cutoff frequency shift from 30.5 to 42 GHz, respectively, as the volume of the air space increased. This effect is important to the interpretation of measured data of the micromachined design.

The measured results of the synthesized filter shown in Fig. 12 indicated an upward shift in the 3-dB cutoff frequency. This shift indicated that the air volume in the filter is larger than expected and is attributed a 20-μm air gap introduced during the application of the conducting epoxy during filter assembly. Inclusion of this additional thin air–space volume ($w * l * h = 2000 \times 4000 \times 20\ \mu\text{m}^3$) underneath the filter into the HFSS simulation[4] produced good agreement between measurement and simulated results, thereby validating the realization of the proposed design approach. The assembly issues encountered in this study can be easily addressed today by using a metal-to-metal bonding technique [8] to eliminate the air gap between the two metal surfaces. In addition, vertical cavities can be realized with the use of deep reactive-ion-etching (DRIE) techniques [9]. Finally, this micromachining approach shows promise for applications at much higher frequencies, such as W-band, where narrow conductor widths can result in unacceptably high ohmic losses.

IV. Conclusions

A micromachined approach has been used to develop synthesized substrates that extend the useful range of high- and low-impedance microstrip values on high dielectric-constant materials. We have realized various low-pass filter designs with either reduced low-impedance or increased high-impedance values on the synthesized substrate sections, and have observed value improvements by a factor of 1.5. The micromachined approach for reducing the low-impedance value has been validated and best impedance improvements occur when the full-thickness conductor width is maintained over the micromachined substrate. Furthermore, in the filter response, sharper rejection band edges have been achieved for increased high-to-low-impedance ratios by a factor of 1.5. In the micromachined approach for increasing the high-impedance value, two primary advantages are observed: 1) reduction in fabrication and design tolerances, which allow for practical realization and 2) reduction of ohmic losses as a result of the wider conducting lines. Successful realization of the high-impedance filter design shows promise for W-band applications, where small conductor dimensions can result in unacceptably high losses. Finally, design and modeling of the structures can be accomplished using commercially available computer-aided design (CAD) tools as well as finite-element method (FEM)-based field simulation solvers.

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